INNA PARTIN-VAISBAND
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ACADEMIC WORK EXPERIENCE

2016 to present **University of Illinois at Chicago, Chicago, Illinois**
Assistant Professor of Electrical and Computer Engineering
- Director of Laboratory for *High Performance Circuits and Systems* (HiPerCAS)
- Research interests: Power efficient ICs/VLSI systems; AI hardware; Hardware Security
- Website: http://innavaisband.wixsite.com/hipercas

2010 to 2016 **University of Rochester, Rochester, New York**
Research Assistant and *Post-Doctoral Researcher*
- Research interests: mixed-signal circuit and system design; distributed locally intelligent power delivery systems; emerging technologies
- Designed, fabricated, and tested a 28 nm, low power management system for Snapdragon chipset (Samsung Galaxy S5) with Qualcomm
- Co-lecturer and teaching assistant
- Website: https://www.rochester.edu

NON-ACADEMIC WORK EXPERIENCE

2015 to 2016 **LexInnova Technologies LLC**
Consultant
- Patent consulting on analog and power delivery circuits for mobile communication technology, part-time
- Website: www.lex-innova.com

2005 – 2009 **R&D, IBM Ltd., Haifa, Israel**
Chip Design Engineer
- Chip design (Xbox 360, PlayStation 3, and others)
- Analyzed IBM design optimization processes and developed a software framework for product validation
- Conducted trainings in IBM Haifa, Israel and IBM Shanghai, China
- Website: https://www.ibm.com

2004 – 2005 **R&D, G-Connect Ltd., Herzeliya, Israel**
Advanced Internet access solutions and value-added-services for service providers and telecommunications network operators
Software engineer
- Responsibilities included prototyping the leading product, enabling enhanced differentiated services in the fields of networking and internet communication (C/C++)
- Designed and developed integrated environment for evaluation and simulation of product features, using C++, VBScript, DOS and UNIX shells
https://www.bloomberg.com/research/stocks/private/snapshot.asp?privcapid=519613

2003 – 2004 **R&D, Tower Semiconductor Ltd. (TowerJazz), Netanya, Israel**
Semiconductor IC design and fabrication services. Main products: RF, HPA, and mixed-signal; power management; non-volatile memory; CMOS image sensor; automotive
EDA/CAD engineer
- Developed and built physical verification environment for Tower's PDK/CAD groups
- Designed tools for report analysis of EDA tools (Calibre/Hercules/Assura), using Perl, Perl/Tk, Shell scripts on Linux and UNIX systems

EDUCATION

2010 – 2015 **University of Rochester, Rochester, New York**
Doctor of Philosophy in Electrical and Computer Engineering
- Dissertation: Power Delivery and Management in Nanoscale ICs

2009 – 2010 **University of Rochester, Rochester, New York**
Master of Science in Electrical and Computer Engineering

2006 – 2009 **Technion – Israel Institute of Technology, Haifa, Israel**
Master of Science in Electrical Engineering

2001 – 2005 **Technion – Israel Institute of Technology, Haifa, Israel**
Bachelor of Science in Computer Engineering, Cum Laude

PUBLICATIONS

Books and Book Chapters

- I. P.-Vaisband and Eby G. Friedman, "Secure Power Management and Delivery within Intelligent Power Networks On-Chip," Green Photonics and Electronics, G. Eisenstein, D. Bimberg, (Eds.), Springer, 2017, ISBN # 978-3-319-67002-7.

- I. P.-Vaisband, R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Köse, and E. G. Friedman, *On-Chip Power Delivery and Management*, 4th Edition, Springer, 2016, ISBN-13: 978-3319293936, ISBN-10: 3319293931.

Journal Papers

- D. Utyamishev and I. P.-Vaisband, "Real-Time Detection of Power Analysis Attacks by Machine Learning of Power Supply Variations On-Chip," *IEEE Transactions on Computer-Aided Design on Integrated Circuits and Systems*, Vol. 39, No. 1, pp. 45–55, January 2020.

- D. Utyamishev, I. Partin-Vaisband, "Progressive VAE Training on Highly Sparse and Imbalanced Data," *arXiv preprint arXiv:1912.08283*, December 2019 (in review in *IEEE TCAD*).

- F. Kenarangi, X. Hu, Y. Liu, J. A. Incorvia, J. S. Friedman, I. Partin-Vaisband, "Exploiting Dual-Gate Ambipolar CNFETs for Scalable Machine Learning Classification," *arXiv preprint arXiv:1912.04068*, December 2019 (accepted for publication in *Scientific Reports*).

- F. Kenarangi and I. Partin-Vaisband, "A Single-MOSFET MAC for Confidence and Resolution (CORE) Driven Machine Learning Classification," *arXiv preprint arXiv:1910.09597*, October 2019 (in review in *IEEE TCAS-I*).

- F. Kenarangi and I. P.-Vaisband, "Exploiting Machine Learning Against On-Chip Power Analysis Attacks: Tradeoffs and Design Considerations," *IEEE Transactions on Circuits and Systems I*, Vol. 62, No. 2, pp. 769–781, 2019.

- I. Vaisband and E. G. Friedman, "Stability of Distributed Power Delivery Systems with Multiple Parallel On-Chip LDO Regulators," *IEEE Transactions on Power Electronics*, Vol. 31, No. 8, pp. 5625–5634, October 2015.

- I. Vaisband, B. Price, S. Köse, Y. Kolla, E. Friedman, and J. Fischer, "Distributed LDO Regulators in a 28 nm Power Delivery System," *Analog Integrated Circuits and Signal Processing*, Vol. 83, No.3, pp. 295–309, March 2015.

- I. Vaisband, M. Saadat, and B. Murmann, “A Closed-Loop Reconfigurable Switched-Capacitor DC-DC Converter for Sub-mW Energy Harvesting Applications,” *IEEE Transactions on Circuits and Systems I*, Vol. 62, No. 2, pp. 385–394, November 2015.
- I. Vaisband and E. Friedman, “Energy Efficient Adaptive Clustering of On-Chip Power Delivery Systems,” *Integration, the VLSI Journal*, Vol. 48, pp. 1–9, January 2015.
- I. Vaisband, M. Azhar, E. Friedman, and S. Köse, “Digitally Controlled Pulse Width Modulator for On-Chip Power Management,” *IEEE Transactions on Circuits and Systems I*, Vol. 22, No. 12, pp. 2527–2534, January 2014.
- I. Vaisband and E. Friedman, "Heterogeneous Methodology for Energy Efficient Distribution of On-Chip Power Supplies," *IEEE Transactions on Power Electronics*, Vol. 28, No. 9, pp. 4267–4280, September 2013.
- I. Vaisband, E. G. Friedman, R. Ginosar, and A. Kolodny “Low Power Clock Network Design,” *Journal of Low Power Electronics and Applications*, No. 1, Vol. 1, pp. 219–246, May 2011 (invited paper).

Conference Papers

- F. Kenarangi, I. Partin-Vaisband, “Security Network On-Chip for Mitigating Side-Channel Attacks,” *ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, pp. 1-6, June 2019.
- I. P.-Vaisband, “Efficient Wireless Power Transfer for Heterogeneous Adaptive IoT Systems,” *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2018.
- I. P.-Vaisband, “Automated Design of Stable Power Delivery Systems for Heterogeneous IoT Systems,” *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2017.
- I. P.-Vaisband and E. G. Friedman, “Passivity-Based Automated Design of Stable Multi-Feedback Distributed Power Delivery Systems,” *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, March 2017.
- I. Vaisband and E. G. Friedman, "Dynamic Power Management with Power Network-on-Chip," *Proceedings of the IEEE International NEWCAS Conference*, June 2014 (nominated for best paper award).
- I. Vaisband and E. G. Friedman, " Power Network On-Chip for Scalable Power Delivery," *Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction*, June 2014.
- I. Vaisband, and E. Friedman, “Computationally Efficient Clustering of Power Supplies in Heterogeneous Real Time Systems,” *Proceedings of the IEEE Symposium on Circuits and Systems*, pp. 1628–1631, May 2014.
- S. Köse, I. Vaisband, and E. Friedman, “Digitally Controlled Wide Range Pulse Width Modulator for On-Chip Power Supplies,” *Proceedings of the IEEE Symposium on Circuits and Systems*, pp. 2251–2254, May 2013.
- I. Vaisband, R. Ginosar, A. Kolodny, E. G. Friedman, “Energy Metrics for Power Efficient Crosslink and Mesh Topologies,” *Proceedings of the IEEE International Symposium on Circuits and Systems* (ISCAS), May 2012.
- I. Vaisband, R. Ginosar, A. Kolodny, E. G. Friedman, “Power Efficient Tree-Based Crosslinks for Skew Reduction,” *Proceedings of the ACM Great Lakes Symposium on VLSI* (GLSVLSI), pp. 285–290, May 2009.

Presentations and Invited talks

- A. Fouman and I. P.-Vaisband, “A Unified Learning Platform for Dynamic Frequency Scaling in Pipelined Processors,” Work-In-Progress Poster at the 2020 Design Automation Conference (DAC), July 2020.
- I. P.-Vaisband, “Learning-Assisted Hardware Security,” at Intel Corporation, Hillsboro, OR, May 2019.
- I. P.-Vaisband, “Learning-Assisted Hardware Security,” Invited talk at the Technion – Israel Institute of Technology, Israel, January 2019.
- I. P.-Vaisband, “Learning-Assisted Hardware Security,” Invited talk at Intel Corporation, Israel, January 2019.
- I. P.-Vaisband, “Secure Power Delivery and Management for Heterogeneous IoT Systems,” Cirrus Logic, Austin, TX, June 2017.
- I. Vaisband, "On-Chip Power Delivery," Invited talk at the Technion – Israel Institute of Technology, Israel, March 2012.
- I. Vaisband, S. Köse, I. Savidis, J. Rosenfeld, and E. G. Friedman, "On-Chip Power Delivery," *CEIS University Technology Showcase*, Rochester, NY, April 2012.
- I. Vaisband, S. Kose, I. Savidis, and E. G. Friedman, “On-Chip Power Delivery," University Technology Showcase, Rochester, New York, April 6 2011.
- I. Vaisband, B. Yeger, I. Granovsky, D. Federovsky, “Reducing Turn Around Time of complicated ECOs – ASIC Design Reutilization,” *Proceedings of the Grace Hopper Celebration (GHC)*, October 2007.

Patents

- I. Vaisband and E. G. Friedman, “Heterogeneous Method for Energy Efficient Distribution of On-Chip Power Supplies and Power Network On-Chip System for Scalable Power Delivery,” United States Patent, No. 9,785,161, October 10, 2017.
- D. Federovsky, D. Kamshitsky, I. Vaisband, and B. Yeger, “Method and System for Reducing Turn Around Time of Complicated Engineering Change Orders and ASIC Design Reutilization,” United States Patent No. 20,090,178,015, July 2009.

HONORS AND AWARDS

- UIC Faculty Award for Advising, 2019
- ACM Recognition of Service Award, SLIP 2019
- Chancellor's Graduate Research Award, 2017
- Sohnis Young Researcher Award – based on achievements and potential for developing an academic career, 2011 – 2012
- IBM Ovation! Award for Axon – cell companion chip development, 2007
- IBM Bravo! Award for delivering the force behind: PlayStation3, 2006

SERVICE ACTIVITIES

External Services

- Associate Editor for *Microelectronics Journal*, since 2015
- Special Session Organizer: "Securing PUFs and Crypto Accelerators Against Machine Learning Based Side-Channel Attacks," *Design Automation Conference* (*DAC*), 2020
- Proceedings Chair: *Great Lake Symposium on VLSI (GLSVLSI)*, 2020
- Guest Associate Editor for *IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE)*; Special Issue on Sustainable Energy through Power-Electronic Innovations in Physical and Cyber Systems, 2020
- Technical Program Chair: *System Level Interconnect Prediction (SLIP) Workshop*, 2019
- Publicity Chair: *Women in Hardware and Systems Security (WISE) Workshop*, 2019
- Technical Program Track Chair: "VLSI Design," *Technical Program of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, 2019
- Technical Program Committee Member: *VLSI Systems & Applications*, since 2017; *IEEE ICCD*, 2019; *IEEE DCAS 2017*
- Special Session Organizer: "Powering Heterogeneous IoT Systems: Design for Efficiency, Security, and Sustainability," *Great Lake Symposium on VLSI (GLSVLSI)* 2019
- Panel Member: "Emerging Trends in On-chip Power Delivery and Management," *ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, 2018
- Session Chair: "Digital Circuits, Systems & Architectures for Machine Learning," ISCAS 2020; "Hardware Security," *ISCAS* 2019; "Digital Design for Deep Learning," ISCAS 2018; "Secure Circuits Design," *ISCAS* 2018; "Low Power Variation Aware Circuit Design," GLSVLSI 2018; "PUF Circuits & Hardware Trojans," *ISCAS* 2018
- Reviewer for scientific journals (JSSC, TPEL, TCAS-I, TCAS-II, TVLSI, TCAD)

Internal (UIC) Services

- Preliminary exam and defense committees (2017–2019)
- PhD qualifying examination "Digital Systems & VLSI Design" and "Power Electronics and Electric Circuits" committee (2017–2019)
- Graduate committee (2018–2019)
- Graduate Adm & Recruitment committee (2019)
- Track chair: "Analog and Mixed-Signal Circuits" (2019)
- Reviewer for DPI-Cycle-I (2019)
- Reviewer for Early Scholar Research Program (ERSP) (2019)
- Reviewer for Projects for Senior Design (2019)
- Reviewer for Provost's Graduate Research Award Program (2018)
- Sole faculty speaker at Women in Engineering Summer Program event (2018)